In the Claims:

Claims 1-2 (canceled).

Claim 3 (currently amended): A memory array comprising:

a plurality of floating gate transistors connected in series,

each floating gate transistor having formed, in a well of a substrate,

a source and a drain region

and

a channel region separating said source and drain regions,

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a dopant concentration region displaced about a target region, said target region situated below said channel region, said dopant concentration region extending into said channel region such that said channel region has a non-uniform concentration of dopant;

wherein said well has a first conductivity type, said source and said drain regions have a second conductivity type, and said dopant concentration region has said second conductivity type.

Claim 4 (previously presented): The memory array of claim 3 wherein said dopant concentration region is formed by a tilted ion implantation utilizing as a mask, at least a part of a gate structure of each floating gate transistor.

Claim 5 (withdrawn): A method for making a memory array comprising:

forming a plurality of floating gate NMOS transistors connected in series, each having a source and a drain region and a channel region separating the source and the drain regions, and

implanting beneath a central portion of the channel region a non-uniform concentration of dopant.

Claim 6 (withdrawn): The method of claim 5, wherein said non-uniform concentration comprises a retrograde concentration distribution in the direction away from the surface of the substrate.

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Claim 7 (withdrawn): The method of claim 6, wherein said non-uniform concentration comprises a lateral distribution along the length of the channel region that is higher in a region generally towards the central portion of the channel region and decreases toward the opposing source and drain regions.

Claim 8 (withdrawn): The method of claim 5, wherein said non-uniform concentration is provided by a tilted ion implantation utilizing as a mask a gate structure of each floating gate transistor.

Claim 9 (currently amended): A transistor comprising:

in a well structure of a substrate, a source and a drain region and a channel region separating said source and said regions, a dopant concentration region displaced about a target region, said target region situated below said channel region, said dopant concentration region extending into said channel region such that said channel region has a non-uniform concentration of dopant;

wherein said well structure has a first conductivity type, said source and said drain regions have a second conductivity type, and said dopant concentration region has said second conductivity type.

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Claims 10-11 (canceled).

Claim 12 (previously presented): The transistor of claim 9 wherein said dopant concentration region is provided by a tilted ion implantation utilizing as a mask, at least part of a gate structure of said transistor.

Claim 13 (previously presented): The transistor of claim 9, wherein the transistor is an NMOS transistor.

Claim 14 (previously presented): The NMOS transistor of claim 13, wherein the NMOS transistor is a floating gate transistor.